



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,788	08/15/2003	Chi-Hsing Hsu	JCLA9912	4789

23900 7590 03/22/2005

J C PATENTS, INC.
4 VENTURE, SUITE 250
IRVINE, CA 92618

EXAMINER

SMITH, BRADLEY

ART UNIT	PAPER NUMBER
----------	--------------

2891

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/643,788

Applicant(s)

HSU ET AL.

Examiner

Bradley K. Smith

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 13-20 is/are allowed.
- 6) ☒ Claim(s) 1,3-5,9,10,21-24 and 26 is/are rejected.
- 7) ☒ Claim(s) 2,6-8,11,12,25 and 27-29 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. ____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☒ Other: search notes.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 3, 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai et al. (US Pregrant Publication 2003/0201521). Tsai et al. disclose a circuit layer on said substrate surface, wherein said circuit layer includes a plurality of first bonding pads (43) and a plurality of second bonding pads (43) on a surface of said circuit layer, at least a die (40) having an active surface and a back side, wherein said die includes a plurality of die pads on said active surface, a plurality of bumps (42), wherein each of said bumps connects one of said die pads with one of said first bonding pads; and a plurality of contacts disposed on said second bonding pads (see figures 3

Art Unit: 2829

and 4). With regards to claim 3, Tsai et al. disclose circuit layer is a patterned conductive layer, which forms said first bonding pads and said second bonding pads (see figures 3 and 4). With regards to claim 4, Tsai et al. disclose plurality of patterned conductive layers, at least a dielectric layer and at least a conductive via, said conductive layers are set on said substrate surface, said dielectric layer is set between said conductive layers, said conductive via penetrating through said dielectric layer (16) electrically connects said conductive layers, and one of said conductive layers farthest from said glass substrate forms said first bonding pads -and said second bonding pads (see figures 4 and 5). With regards to claim 5, Tsai et al. disclose the contacts are balls. However Tsai et al. fails to disclose the use of the glass substrate. Whereas the applicant disclosed in the background of his own invention that it is well substrates include ceramics (glass). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a glass substrate because the alternative (organic substrate) cannot meet the bond pad density requirement (specification page 3 lines 5-12).

5. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai et al. (US Pregrant Publication 2003/0201521) as applied to claim 1 above, and further in view of Macric (US 2002/0033189). Tsai et al. disclose the chip package *supra*. However Tsai fail to disclose a heat spreader on the backside of the substrate. Whereas Macric disclose a heat spreader on the back side of the substrate (figure 2). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Tsai and Macric in order to dissipate

heat that builds up in the chip structure which could alleviate overheating issues, and enable more active device to be packaged.

6. Claims 21-24, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai et al. (US Pregrant Publication 2003/0201521). Tsai et al. disclose, a circuit layer on said substrate surface, wherein said circuit layer has an interconnection structure; at least a die on said circuit layer, wherein said die is coupled to said interconnection structure; and a plurality of contacts on said circuit layer, wherein said contacts are coupled to said interconnection structure (see figures 4 and 5). With regards to claim 22 Tsai et al. disclose the circuit layer is the patterned conductive layer. With regards to claim 23, Tsai et al. disclose plurality of patterned conductive layers, at least a dielectric layer and at least a conductive via, said conductive layers are set on said substrate surface, said dielectric layer is set between said conductive layers, said conductive via penetrating through said dielectric layer (16) electrically connects said conductive layers, and one of said conductive layers farthest from said glass substrate forms said first bonding pads -and said second bonding pads (see figures 4 and 5). With regards to claims 24 and 26, Tsai et al. disclose the use of flip chip technology the contacts are balls. However Tsai et al. fails to disclose the use of the glass substrate. Whereas the applicant disclosed in the background of his own invention that it is well substrates include ceramics (glass). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a glass substrate

because the alternative (organic substrate) cannot meet the bond pad density requirement (specification page 3 lines 5-12).

Allowable Subject Matter

7. Claims 13-20 are allowed.
8. Claims 2, 6-8, 11, 12, 25, 27-29 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
9. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record neither teaches nor fairly suggest within the context of the entire claim the insulating layer between the circuit layer and the die (claim 2), a chip package with an active or passive device within the circuit layer (claims 6-8 and 27-29), heat conducting layer connecting to the contacts (claims 11 and 12) wire bonding (claim 13-20 and 25).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bradley K. Smith whose telephone number is (571) 272-1884. The examiner can normally be reached on 10-6 Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Balmiest can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2829

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Brad Smith', is positioned above the printed name.

Brad Smith
Primary Examiner
Art Unit 2829